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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/814,421	03/31/2004	Stephen Wu	BP 3117	5685	
51472 7	590 01/25/2006		EXAMINER		
GARLICK HARRISON & MARKISON LLP			. WILSON, ALLAN R		
P.O. BOX 160' AUSTIN, TX			ART UNIT	PAPER NUMBER	
,			2815		
			DATE MAILED: 01/25/2006	DATE MAILED: 01/25/2006	

Please find below and/or attached an Office communication concerning this application or proceeding.

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		Application No.	Applicant(s)			
Office Action Summary		10/814,421	WU ET AL.			
		Examiner	Art Unit			
		Allan R. Wilson	2815			
Period fo	The MAILING DATE of this communication ap or Reply	pears on the cover sheet wit	h the correspondence address	•		
A SH WHIC - Exte after - If NC - Failu Any	ORTENED STATUTORY PERIOD FOR REPL CHEVER IS LONGER, FROM THE MAILING D insions of time may be available under the provisions of 37 CFR 1.1.2 SIX (6) MONTHS from the mailing date of this communication. O period for reply is specified above, the maximum statutory period are to reply within the set or extended period for reply will, by statute reply received by the Office later than three months after the mailing ed patent term adjustment. See 37 CFR 1.704(b).	DATE OF THIS COMMUNIC 136(a). In no event, however, may a re will apply and will expire SIX (6) MONT te, cause the application to become AB	CATION. sply be timely filed IHS from the mailing date of this communicat ANDONED (35 U.S.C. § 133).			
Status						
1)⊠	Responsive to communication(s) filed on <u>02 N</u>	<i>May 2005</i> .				
2a)□	This action is FINAL . 2b)⊠ This	s action is non-final.				
3)□	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is					
	closed in accordance with the practice under	Ex parte Quayle, 1935 C.D.	. 11, 453 O.G. 213.			
Disposit	ion of Claims					
4)⊠	Claim(s) 1-20 is/are pending in the application	า.				
	4a) Of the above claim(s) is/are withdra	awn from consideration.				
5)⊠	Claim(s) <u>1-15</u> is/are allowed.					
	Claim(s) <u>16-20</u> is/are rejected.					
•	Claim(s) is/are objected to.					
8)[]	Claim(s) are subject to restriction and/o	or election requirement.				
Applicat	ion Papers					
9)[The specification is objected to by the Examine	er.				
10)[The drawing(s) filed on is/are: a) acc					
	Applicant may not request that any objection to the	- · ·	·			
441	Replacement drawing sheet(s) including the correct	•	•			
11)[_]	The oath or declaration is objected to by the E	xaminer. Note the attached	Office Action or form P10-152.	•		
Priority (under 35 U.S.C. § 119					
	Acknowledgment is made of a claim for foreign All b) Some * c) None of:	n priority under 35 U.S.C. §	119(a)-(d) or (f).			
۵,	1. Certified copies of the priority document	its have been received.				
	2. Certified copies of the priority document		oplication No			
	3. Copies of the certified copies of the price	ority documents have been	received in this National Stage			
	application from the International Burea	au (PCT Rule 17.2(a)).				
* 5	See the attached detailed Office action for a list	t of the certified copies not r	eceived.			
Attachmen		🗖	(DTO			
	ce of References Cited (PTO-892) te of Draftsperson's Patent Drawing Review (PTO-948)		ummary (PTO-413))/Mail Date			
3) 🔲 Infon	mation Disclosure Statement(s) (PTO-1449 or PTO/SB/08) or No(s)/Mail Date	· ·	formal Patent Application (PTO-152)			

DETAILED ACTION

Claim Objections

Claims 1, 8 and 17 are objected to because of the following informalities:

Claim 1 ends in a semicolon.

Claim 8 recites the limitation "each well region" in line 1. There is insufficient antecedent basis for this limitation in the claim. Should probably depend on claim 7.

Claim 17 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. The MOSFET transistor configured as a capacitor is in claim 16.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 16-20 are rejected under 35 USC § 102(b) as being anticipated by U.S. Patent No. 4,570,331 to Eaton, Jr. et al. ("Eaton").

With regards to claims 16 and 17, Eaton illustrates in figures 1a-5 (entire document) a plurality of n-well regions 16 (FIG. 3), within a p-substrate material 10; and wherein each of the

n-well regions comprises at least one of a MOSFET transistor 38 (FIELD SHIELD ISOLATION TRANSISTOR) configured as a capacitor and a metal layer capacitor 18, 20, 22 (col. 4, lines 5-18) formed on top of each of the n-well regions.

With regards to claims 18-20, Eaton discloses in col. 4, lines 17-18, the MOSFET transistor configured as a capacitor is coupled between supply 16 and ground 22.

Allowable Subject Matter

Claims 1-15 are allowed provide the objections above to claims 1 and 8 are overcome.

The following is an examiner's statement of reasons for allowance:

A close prior art, U.S. Patent No. 4,959,650 to Moyal, discloses most of the limitations of the claims, but fails to show at least a metal fill portion, a MOSFET capacitor or a metal layer capacitor.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Hseuh (illustrates a transistor having a capacitive network), Hershbarger et al. (illustrates capacitors at a high voltage barrier); Scott et al. and Hein et al. (illustrate capacitors between two circuits); and Poh (illustrates a layered capacitor on a well).

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Any inquiry concerning this communication or earlier communications from an examiner should be directed to Primary Examiner Allan Wilson whose telephone number is (571) 272-1738. Examiner Wilson can normally be reached 7:00-4:00 Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Allan R. Wilson Primary Examiner 23 January 2006